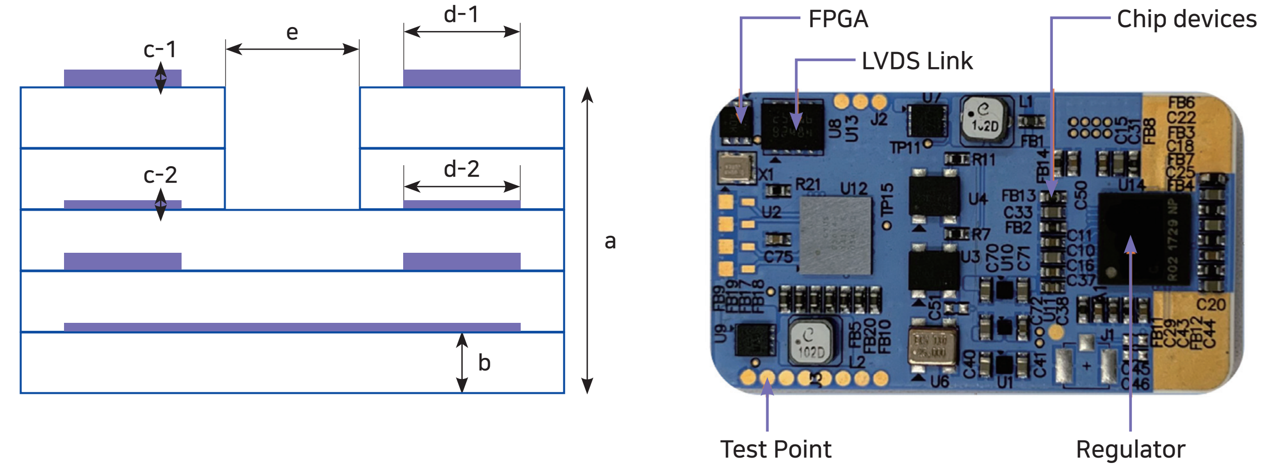
Design Rules for AiP

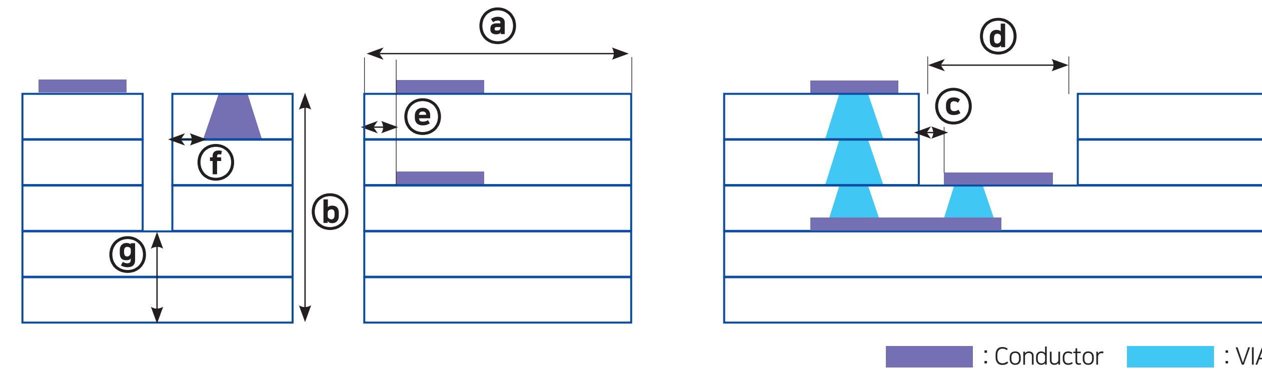
Design rules for modules which include AiP(Antenna in Package) and other package modules.
This picture is example of AiP after plating and mounting BFIC chips.



Design Feature	Rule		Tolerance
Substrate Size	≤ 110 SQ		± 0.5% + Cutting tolerance(0.1mm) Ex) 50mm x 50mm(50*0.5%)mm + 0.1mm = 0.35mm
(a) Substrate Thickness	**0.8 ~ 2.5 mm (Without conductor thickness)		± 5%
(b) Dielectric Thickness	Adjustable in 0.05mm increments. Ex) 0.05, 0.1, 0.15mm		± 5%
(c) Conductor Thickness	c-1 Outer	Ag 0.01mm + Plating(Ni 2~5um + Au 0.02~0.1um) *1um = 0.001mm	
	c-2 Inner	Ag 0.007mm	
Conductor Layer Count	Max. 31 layers		
(d) Pad Size	d-1 Outer => Min. 0.13mm		± 7.5%
	d-2 Inner => Min. 0.1mm		
(e) Cavity Dimension	Min. 1mm		± 0.1mm
Camber	Different standard depending on the size of the board. Up to 30mm x 30mm => less than 0.1mm Up to 50mm x 50mm => less than 0.15mm Up to 110mm x 110mm => less than 0.2mm		

*YL-5W is suited for applications with operating frequencies for mm-Wave **AiP(Antenna in Package)**, modules and chip components. Testing has been performed up to 90 GHz with outstanding results.
**YL-8W is designed for resistance device, communication parts.

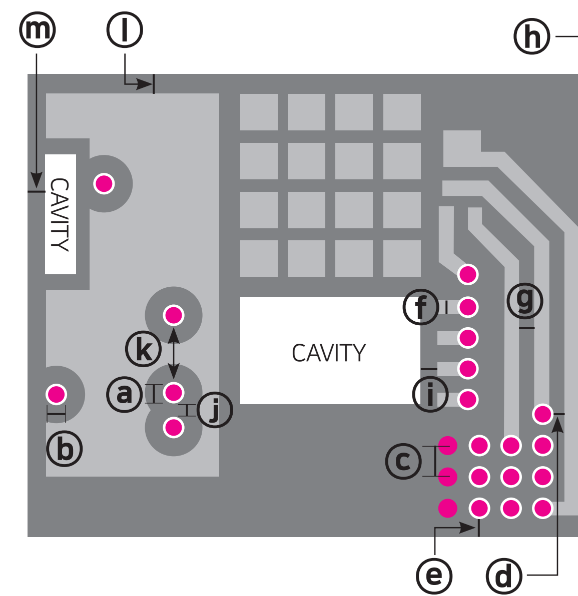
Design Rules for AiP



No	Basic structural sizes	Rule
ⓐ	Sub. Edge to Cavity Edge	Min. 1
ⓑ	Max. cavity height	Max. 2.5
ⓒ	Cavity shelve edge - conductor spacing	Min. 0.1

No	Basic structural sizes	Rule
ⓓ	Min. cavity width	Min. 1
ⓔ	Conductor-cavity spacing	Min. 0.1
ⓕ	Via cavity spacing	Min. 0.2
ⓖ	Cavity bottom thickness	Min. 0.7

Unit : mm



*Standard Via Diameter is 0.1mm for tape layer 0.1mm thickness and other Via Diameter such as 0.08 ~ 0.25 can specified by consultation with Y-Tech engineers.

No	Basic structural sizes	Rule
ⓐ	Via Diameter*	0.05~0.3
ⓑ	Cover Pad Diameter	Min. 1.4*a
		Outer Min. 0.13
		Inner Min. 0.07
	Ex) Via : 0.05, Cover pad : 0.07 Via : 0.10, Cover pad : 0.14	
ⓒ	Via Pitch	Min. 2.5*a
ⓓ	Via Pad to Line	Min. 0.1
ⓔ	Via Pad to Substrate Edge	Min. 0.3
ⓕ	Line Width	Outer Min. 0.12
		Inner Min. 0.08
ⓖ	Line Spacing/DC Pad Spacing	Min. 0.09
ⓗ	Pattern to Substrate Edge	Min. 0.3
ⓘ	Line to Cavity Edge	Min. 0.1
ⓙ	Isolation Gap	Min. 0.07
ⓚ	Solid Plane	Min. 0.1
ⓛ	Sub. Edge to GND Plane/DC Pad	Min. 0.3
ⓜ	Cavity Edge to GND Plane/DC Pad	Min. 0.3

Unit : mm

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Y-TECH LTCC DESIGN RULES FOR AiP

Material Properties

Specifications	Units	*YL-5		**YL-8	YL-20	YL-40
Dielectric Constant	-	1MHz	60GHz	1MHz	6GHz	6GHz
		6.2	5.9	8.3	19.6	42.5
Loss Tangent	-	0.0009	0.002	0.0038	0.0012	0.0005
Thermal Co-efficient Expansion	ppm/°C	5.7		7.1	10	15
Thermal Conductivity	W/mK	2.2		2.5	7.6	3.4
Thermal Conductivity For Thermal Via	W/mK	20				
Flexural Strength	MPa	>200		>260	>200	>200
Conductor Material	-	Ag		Ag	Ag	Ag
Plating	um	Ni : 2~5 Au : 0.02 (If wire-bonding is required Au 0.1)				

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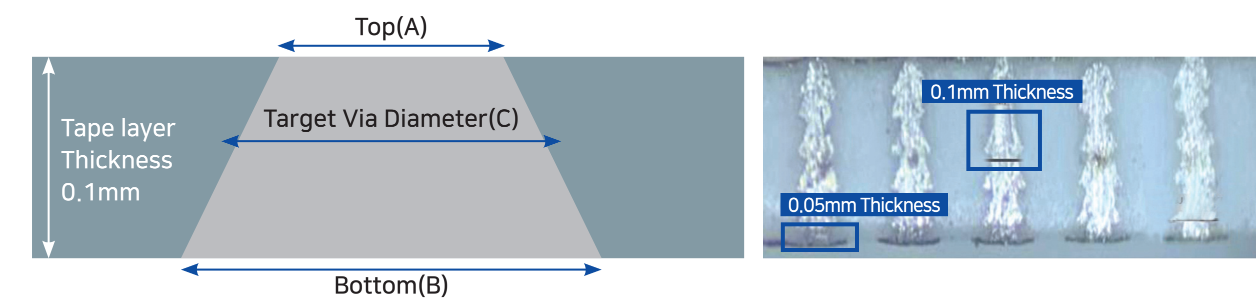
Via

The laser forming via can create the ground vias as well as the registration holes. The inlet surface on which the laser is directly emitted is larger than the outlet surface because of the laser focus.
General tape layer thickness is 0.05 and 0.1mm after sintering. 0.15 and 0.2 are optionally possible.
Based on a 100um thickness sheet, It has a deviation of ±5um compared to the original size. The surface perforated by the lazer is larger than where the laser exits. Via size ±10um is the tolerance of position represented by the dotted line on the picture.
When the via size is 100um, the via size of dotted line is between 120um(Top) to 80um(Bottom).



Location	Target Via Diameter(C)			
	*0.08	0.1	0.15	0.2
A	0.06	0.08	0.13	0.18
B	0.1	0.12	0.17	0.22

Unit : mm

Shrinkage Consideration

Side view of the board

Before Firing After Firing

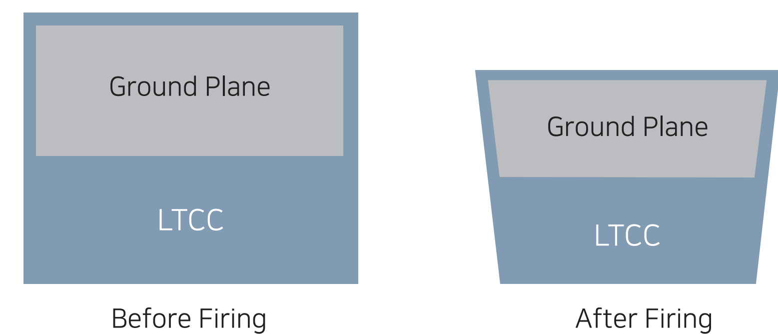
If the distribution of the metal in the layer is not balanced, serious warpage may occur after sintering.
In Figure A, the metal is concentrated locally and non-uniformly only on the upper part. This type of metal arrangement causes the product to bend after sintering.
Figure A' is an exaggerated example of A after sintering.

Side view of the board

Before Firing After Firing

Figure B, on the other hand, has a uniform distribution of metal, both up and down.
In this case, the product shrinks uniformly and warpage is significantly reduced when compared to A.
It can be noted that the uniformity of the metal distribution affects the warpage.

Top view of the board

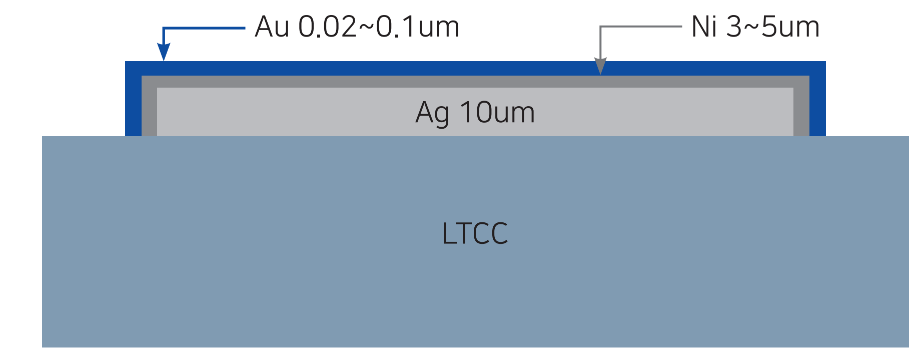


Before Firing After Firing

If the metal coverage, such as ground plane, is not balanced, it can result in differential shrinkage issues.
As mentioned earlier, the distribution of metal should be uniform. This applies to both the inter-layer distribution and the area-to-area distribution.

Plating

General thickness of Au plating is Min. 0.02um.
If wire-bonding is required, the thickness of the gold can be as thick as 0.1mm.



Solder Resist(SR)

Solder Resist (SR) is printed after conductor print to achieve SMT precision. Unlike the PCB structure where SR is applied on top of metal, LTCC connects vias and conductor patterns and covers the SR.
Since the SR is printed between conductor patterns, these are occasionally smeared due to conductor irregularities.
Therefore the gap between solder resist and conductor should also be taken into account when designing SR.
It is recommended to give a tolerance of about 100um at the end of the conductor pad.